SPRIN-D

BUNDESAGENTUR
FÜR SPRUNGINNOVATIONEN

A SEMICONDUCTOR STRATEGY FOR THE EUROPEAN UNION

SUMMARY OF THE ANALYSIS AND PROPOSAL FROM THE AGENCY FOR DISRUPTIVE INNOVATION MULTINATIONAL WORKING GROUP - SEP 6TH 2021

The European Union's (EU) economy is confronted to the dependence on Asian and US actors, dependence that is mainly caused by the lack of industrial capabilities in several domains. The EU is therefore increasingly working to strengthen its technological sovereignty. We argue for a strategy towards technological sovereignty in the field of semiconductor that focuses on:

a) research and development for new semiconductor products,
b) capacities for R&D pilot line manufacturing of advanced and leading node-size chips in close collaboration with foundry high-volume manufacturing to promote the EU industry and strengthen its technological sovereignty (e.g., its value chain),
c) competencies for new manufacturing processes and computing-intensive architectures for advanced cloud and edge computing, automotive, 5/6G, health and other industrial applications,
d) advanced packaging,
e) hardware support for high-performance computing for defense, research and industry.

NEW SEMICONDUCTOR PRODUCTS

Positioning the EU industry to compete for the best semiconductor products in future requires major efforts, because autonomously acting systems such as in autonomous electric vehicles or industrial robots and the communications infrastructure for 5G/6G will require completely new chip technologies. Central elements of these systems are microprocessors and controllers that process enormous amounts of data with maximum energy efficiency and also have to meet protection against attacks and requirements for fail-safety.

The majority of today's microprocessors and controllers is based on the IP of the British company ARM, which licenses its designs to chip manufacturers worldwide, the so-called ARM architecture. This ARM architecture is characterized by high processing speeds with relatively low power requirements and has therefore established itself as a quasi-standard over the last 30 years. As a result, many manufacturers worldwide are heavily dependent on ARM. It therefore generally makes strategic sense to establish an EU alternative in order to keep dependencies in the EU as low as possible. This alternative is offered by the RISC-V instruction set architecture, which is available worldwide as an open-source license. This architecture would have the advantage that it can be adapted relatively easily to the needs of specific product requirements compared to the ARM architecture. However, the substantial shift of the local

chip industry to the RISC-V instruction set architecture requires a long-term strategy. An extensive ecosystem with corresponding competencies in the form of patents, peripherals, libraries, and know-how must be built up that is comparable to the ecosystem of the ARM architecture.

A 3-NM CHIP FOUNDRY

It can be assumed that autonomous driving will completely change the industry through disruptive product and service offerings and that the demand for high-performance chips with structure widths around 3 nm could substantially exceed today's forecasts. Tesla has recently proved that centralized architectures based on 8-nm chips can dramatically simplify the architecture of a car. If the current semiconductor supply chains are not fundamentally changed, this potentially huge demand will drastically increase the EU's dependence on Asian manufacturers in the future. Not only in the field of autonomous vehicles, but also in the development of products with artificial intelligence, in Industry 4.0, 5G/6G, and in the Internet of Things, EU-based companies will only be able to develop future products and services in coordination with Asian manufacturers. This coordination could lead to significant delays and to an outflow of high-tech knowledge from the chip developers to the chip manufacturers in Asia. Moreover, it will be impossible for the EU research institutions to access suitable pilot lines and decades of advanced know-how will be simply lost. However, it has to be emphasized that the need of the EU's industry for such high-end production technologies is difficult to forecast. Nonetheless, there might be industrial benefits for the establishment of an advanced foundry in Europe.

In spite of a large industrial community in the EU, none of the EU's semiconductor manufacturers is in the global top 10 (Gartner, 2021). Also, none of the aforementioned EU companies has the size to invest in a competitive 3-nm facility. An ASML 2-nm lithography equipment costs 0,5 billion EUR and one complete line exceeds 1 billion EUR. Moreover, let alone the technology development cost, the required investment would require the equivalent of about one year of combined revenues of the three major EU players and would drain all their resources from the existing roadmap (that has to be preserved and reinforced thanks to the microelectronics IPCEI already underway). An alliance with a non-EU partner and ecosystem is therefore mandatory to have a 3-nm manufacturing facility in the EU.

A factory for chips with structure widths of 3 nm and below will reduce economic dependencies and mitigate geopolitical risks. An EU-based foundry would bring extensive advantages for the EU semiconductor industry. On the one hand, such investment will result in a technology transfer in the form of machines and systems that will henceforth be available to EU industry and research community. On the other hand, significant knowledge gains can be expected through cooperation in research on semiconductor technology in the form of spillover effects (such as the transfer of knowledge about mRNA technology from BioNTech to Pfizer) and an increase in skilled workers. The demand for skilled workers will be met by the influx of corresponding competence carriers and the expansion of educational offers on the part of universities and companies, which will further strengthen the position of the EU. In the current decade, capacities and competencies could thus be built up in order to minimize the technological backlog of the EU in semiconductor production and to regain a substantial part of the

technological sovereignty, also by expanding the control points of the EU Industry on the semiconductor supply chain, which today is limited to ASML. The emerging semiconductor ecosystem will strengthen the ability of EU chip developers to design high-performance chips in future. These chip developers can then use the foundry's production capacities directly on site and thus reduce uncertainties currently prevailing in their supply chains.

NEW MANUFACTURING PROCESSES

Several research institutions in the EU provide leading-edge competencies for enablement of the silicon manufacturing processes, namely CEA-LETI (FR), IMEC (BE), and Fraunhofer 300-mm-based institutes (DE). It is of high-importance to better bundle these research capacities and define a common approach with well-defined focus areas per partner. This cooperation would drive research on semiconductor process technology for application domains mainly served by European industries, from current node size down to leading node size structures. Beside and complementary to transistor architecture, memories and 3D architecture will be a key issue and should be encompassed within the European global approach.

Today, almost all digital chips rely on classical von Neumann architectures, in which 90% of power consumption is due to data manipulation between computing and memory cores. Embedded non-volatile memory are required to reduce drastically the energetic cost of memory access, which is all the more important for applications requiring a lot of data handling, like AI. Intensive R&D will be necessary to mature these technologies and should be a subject of cooperation. In addition to advanced memory, in-memory computing technology is expected to very significantly reduce circuits' power consumption, either using classical static random-access memory and/or non-volatile memory.

Advanced packaging for high density of interconnection requires 1) a technology offering a very fine pitch, and 2) a technology able to assemble Known Good Dies to optimize the total cost of fabrication. Chip-to-wafer technology combines reliable direct hybrid bonding and self-alignment to increase the manufacturability. It is expected to be efficient to assemble chips made at very small nodes. Combined with direct copper bonding, this technology is intended to provide a unique solution for very fine pitch SoC. Advanced packaging for heterogenous integration allows the integration of different functionality on a same SoC. 3D integration to interconnect the chips between each other without using wires, by stacking them on each other just before the end of their fabrication allows designing new systems combining several functions and optimizing their global performances.

Advanced packaging for complex SoC mandates for high level of parallelism, but also to combine various technology nodes. Innovative 3D chiplet integration opens a new way to enhance complex SoC functionality. This technology aims at assembling several chips, fabricated separately, and interconnect them on a same active interposer.

In order to support the EU industrial ecosystem and national sovereign needs on the longer term, any leading edge fab in EU will have to be complemented by a local associated collaborative research plan. The outlined R&D topics will require accompanying investments to upgrade/extend the existing 300 mm R&D facilities in order to reach the necessary technology capability as well as by supporting actions in modelling, design, design tools and architectures.

These complementary steps will be detailed at a later stage as they will heavily depend on the choices made on the program. We see three major axes in the R&D plan:

1. Technology developments required for adapting pure digital technology to the Automotive, 6G, Industrial and Health needs

A first action, would be to create links with the major EU industrial players to define, in advance, the major specifications and requirements for declinations of the basic technology for their applications. A critical element required for a wide usage of a technology node outside the pure digital domain is the availability, in its offering, of I/O capable of driving outside peripherals and hence the capability of having at least 3.3V or 5V capability on some pins. Another one is to have devices with excellent properties in terms of matching and linearity to integrate some analog functions together with the digital ones.

Another action will be the development of dedicated heterogeneous integration schemes to add specific devices. These techniques will open up optimization paths for the designers when addressing system partitioning. An important component for the above-mentioned fields of application id the availability of embedded non-volatile memories.

Always targeting Automotive and 6G, the need of beyond state-of-the-art solutions with much improved energy efficiency for high-workload processors (CPU, GPU, AI accelerators) is a major requirement already by the end users.

2. Complements to and evolution for advanced nodes technology for its extension in time

The above initiatives cannot be considered a one shot and will require extension to insure the longest possible application of the said technologies. In this respect, we propose to conduct research on major topics required by the evolution of the devices, notably transition to 3-D cells structures, introduction of larger amount of high-density memory (and eventual replacement of static random-access memory) and evolution of the 3D assembly and packaging towards much denser pitches and new integration schemes.

To further extend the miniaturization and reduce the power consumption at system level, a major axis will the development of tailored chiplet solutions for the needs of different applicative sectors (high-performance computing, Automotive, 6G).

3. New devices and architectures for ‘beyond gate-all-around’

Another critical research path will be towards upstream research in materials, devices and architectures. 2-D materials will be jointly developed in 300 mm and investigated for applications to backend memories and reconfigurable interconnects.

ADVANCED PACKAGING

Beside the foundry it is part of the plan to install a fab for advanced packaging in order to balance the backend capacity with the increased chip demand and wafer production. A packaging fab with its technology could be supported by research and development via research cooperation. Typical packaging configurations have included the 2-D integrated-circuit technologies such as wafer-level, flip-chip, and through silicon via setups. The early adopters will

need to invest significantly in the ecosystem—hiring new engineers, for instance, or spending the time and money to establish partnerships. They will also need to find cost-effective ways to upgrade their equipment to handle newer through-silicon via-based technologies and processes. In some cases, existing 2-D integrated circuits machinery can be expanded to meet newer capacity requirements. But integrated-circuits manufacturers and foundries may also need to purchase and install new equipment for, say, through-silicon via-based etching or copper filling. Integrated-circuits manufacturers and foundries could also address this need by entering into partnerships with equipment manufacturers to codevelop bonding, plating, and reveal capabilities that they may not have.

HIGH-PERFORMANCE COMPUTING

The European Council has approved a financing proposal for the EuroHPC (High-Performance-Computing) project, which provides almost 7 billion euros for the new construction and expansion of EU supercomputers. The first round of applications for funding from the budget will start this year. Currently, the European Union does not produce high-end processors that can reach the performance levels required for world-class supercomputers. The EuroHPC will therefore launch own research and innovation programs for the development of high-end European technologies, for example in the European Processor Initiative.

Leonardo will be one of eight pre-exascale supercomputers that will form the EuroHPC European high-performance computing network and will be built in Italy, at the Bologna technopole. Initially planned for early 2021, but entry into operation has been delayed towards the end of the same year.

While this program is under development, the EU can accelerate the availability of an Exascale facility by 2024 through a cooperation with a non-EU partner. This center would serve the EU defense industry as well as other research and business institutions requiring access to state-of-the-art computing before the EuroHPC, granting access to all the EU players who require HPC now (medical research first).